This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously cancelled).

2. (Previously cancelled).

3. (Previously cancelled).

4. (Previously cancelled).

5. (Previously cancelled).

6. (Previously cancelled).

7. (Previously cancelled).

8. (Previously cancelled).

9. (Currently amended) A semiconductor chip package, comprising:

a lead frame including a frame body, at least two chip-receiving windows formed in said frame body, a plurality of internal connection leads formed on said frame body adjacent to said chip-receiving windows, and a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows; and

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads formed thereon, wherein said internal connection leads are electrically connected to said bonding pads on said at least two integrated circuit chips in said at least two chip-receiving windows to establish internal electrical connection among said at least two integrated circuit chips, wherein one of said integrated circuit chips [~~in at least one of said chip-receiving windows~~] is a master integrated circuit chip, and another of said integrated circuit chips [~~in other one of said chip-receiving windows~~] is a slave integrated circuit chip, wherein said master integrated circuit chip includes an embedded testing circuit to permit testing of said slave integrated circuit chip that is connected thereto during a testing process of said semiconductor chip package[~~; and~~

~~wherein said external connection leads are electrically connected to said bonding pads other than to bonding pads on said slave integrated circuit, said external connection leads serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said chip receiving windows is established via said external connection leads~~].

10. (Currently amended) The semiconductor chip package as claimed in Claim 9, wherein said internal connection leads are wire-bonded to said bonding pads on said at least two integrated circuit chips in said at least two chip-receiving windows.

11. (Currently amended) The semiconductor chip package as claimed in Claim 9, wherein [~~said~~] there are no external connection leads

[~~are wire bonded~~] electrically connected to [~~said~~] any bonding pads on said slave integrated circuit chip, said external connection leads serving as terminal pins such that external electrical connection with said slave integrated circuit chip is established only via said master integrated circuit chip [~~chips in said chip receiving windows~~].

12. (Currently amended) The semiconductor chip package of Claim 9, wherein[~~, during~~] for the testing process of said semiconductor chip package, said master integrated circuit chip is configured to receive stimulating signals via said external connection leads to stimulate said at least one slave integrated circuit chip via said internal connection leads in response to the stimulating signals, to receive stimulation response of said at least one slave integrated circuit chip via said internal connection leads, and to output information corresponding to the stimulation response via said external connection leads.